Amendments to the Drawings

The attached sheet includes changes to Fig. 3. This sheet, which includes Fig. 3, replaces the original sheet including Fig. 3.

Attachment: Replacement Sheet.

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-8, 10, 12-14, 15-30, 32, 35, 35, 37-44, and 48 are presently active. Claims 9, 11, 14, 31, 33, 36, 45-47, and 49-51 have been canceled. Claims 1, 12, 13, 23, 34, 35, 38, 39, and 48 have been presently amended.

In the outstanding Office Action, Claims 1-8, 10-30, 32-44, and 48-50 were rejected under 35 U.S.C. § 112, first paragraph, as based on a disclosure which is not enabling. Claims 1-8, 10-30, 32-44, and 48-50 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al, in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al and further in view of U.S. Pat. No. 6,263,255 to Tan et al.

Regarding the 35 U.S.C. 112, first paragraph, rejection: Applicants acknowledge with appreciation the courtesy of Examiner Saxena to interview the related case U.S. Serial No. 10/673,138 with Applicants' representative and with one of the named inventors. During that interview, claim changes similar to that submitted herewith and arguments for patentability were discussed. Specifically, the claims (as amended) address the 35 U.S.C. § 112, first paragraph, rejection by providing details such that no undue experimentation would be required for a person of ordinary skill in the art to practice the invention. Below is a claim chart showing the elements of Claim 1 and illustrative passages from Applicants' published application (referred to by the published paragraph numbers).

Claim 1	**Support in Applicants' Published Application for Amendments**
1. A method of facilitating a process performed by a semiconductor processing tool, comprising: inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool	Numbered paragraph [0037] states: For example, the physical model 106 may include a spatially resolved model of the physical geometry of the tool 102, which is different, for example, for a chemical vapor deposition (CVD) chamber and a diffusion furnace. Numbered paragraph [0042] states: In addition to inputting the input data, the first principles simulation processor 104 also inputs the first principles physical model 106 as shown by step 203. Step 203 includes inputting the physical attributes of the tool modeled by the model, as well as first principles equations codified in software necessary to perform a first principles simulation of a desired attribute of the process performed by the semiconductor processing tool 102. Numbered paragraph [0096] states: For the exemplary system of FIG. 13, the model executed on the simulation module can, for example, include three components, namely, a thermal component, a gas dynamic component, and a chemistry component. In the first component, the gas-gap pressure field can be determined, followed by a calculation of the gas-gap thermal conductance. Thereafter, the spatially resolved temperature field for the substrate (and substrate holder) can be determined by properly setting boundary conditions (and internal conditions) such as boundary temperature, or boundary heat flux, power deposited in resistance heating elements, power removed in cooling elements, heat flux at substrate surface due to the presence of plasma, etc.)
and 2) a grid set addressing the	Numbered paragraph [0076] states:

semiconductor processing tool or a geometry of the semiconductor processing tool;	The grid database 618 can include one or more grid sets, whereby each grid set addresses a given process tool or process tool geometry. Each grid set can include one or more grids with different grid resolutions, ranging from coarse to fine. The selection of grids can be utilized to reduce solution time by performing multi-grid solution techniques (i.e. solve for a simulation result on coarse grid, followed by solution on finer grid, finest grid, etc.).
inputting process data related to an actual process being performed by the semiconductor processing tool; setting ~~initial and~~ boundary conditions for [[a]] the spatially resolved model of [[a]] the physical geometry of the semiconductor processing tool based on said process data related to the actual process being performed by the semiconductor processing tool;	Numbered paragraph [0096] states: Thereafter, the spatially resolved temperature field for the substrate (and substrate holder) can be determined by properly setting boundary conditions (and internal conditions) such as boundary temperature, or boundary heat flux, power deposited in resistance heating elements, power removed in cooling elements, heat flux at substrate surface due to the presence of plasma, etc.)
storing in a fab-level library known simulation results obtained from simulation modules in a device manufacturing fab and distributing the known simulation results to other semiconductor processing tools in the device manufacturing fab;	Numbered paragraph [0048] states: The fab-level library 310 is a database for storing simulation results obtained from any of the simulation modules of the network system. Numbered paragraph [0049]: The network architecture of FIG. 3 provides the ability to distribute model results done at one processing tool 102 for one condition set, to other similar or identical tools operating later under the same or similar conditions. Figure 3
solving the computer-encoded differential equations of the first principles ~~simulation~~ physical model for the spatially	Self evident

resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed by:	
using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and	Numbered paragraph [0049] states: Complex simulations requiring greater computational resources may be executed using code parallelization techniques on multiple simulation modules in the network that may be on-tool or standalone.
re-using known simulation solutions as initial conditions for the first principles simulation,	Numbered paragraph [0050] states: Reuse of the known solutions as initial conditions for first principles simulation reduces the computational requirements and facilitates the production of simulated solutions in a time frame consistent with on-line control.
wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module;	Numbered paragraph [0076] states: When the simulation module 606 retrieves the tool data for a given process run, the library 610 can be searched based upon model input to determine the closest fitting solution. This solution can be used according to the present invention as an initial condition for subsequent first principles simulation, thereby reducing the number of iterations required to be performed by the simulation module to provide a simulation result.
providing ~~a first principles simulation result~~ from the solution of the computer-encoded differential equations solved concurrently with the actual process being performed a first principles simulation result; and	Self evident

using the simulation result as part of a data set that characterizes the actual process being performed by the semiconductor processing tool.	No change

Thus, the 35 U.S.C. § 112, first paragraph, rejection has been overcome without adding new matter.

Regarding the art rejection: In light of the new evidence attached herewith, the pending claims as clarified patentably define over the applied art for the following reasons.

The examiner relies on col. 7, lines 21-35, of Sonderman et al for an asserted teaching of setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool. See Office Action, page 16, lines 20-22. Yet, col. 7, lines 21-35, of Sonderman et al ***merely*** describes:

> Turning now to FIG. 5, a flowchart representation of the steps for performing the process simulation function described in block 440 of FIG. 4 , is illustrated. The system 100 prepares one or more process models for simulation (block 510). The models that are prepared for simulation may include the device physics model 310, the process model 320, and the equipment model 330. The number of models defined by the system 100 generally depends upon the interactions of model-components that are to be examined by the simulator 340. In other words, the system 100 determines which components in a model are to be modified and which components are to be monitored for reactions caused by the original component modification. One embodiment of a flowchart depiction of the steps of preparing the processing models for simulation is illustrated in FIG. 6

There are no details here of a first principles physical model including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool and 2) a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool.

The outstanding Office Action relies on Jain et al for an asserted teaching of "solving the computer-encoded differential equations of the first principles simulation model" using

Jain et al's MPE engine. Applicants previously pointed out that Jain et al describe at pages 372-373 (reproduced below) the development of ***futuristic*** computational equipment:

> We ***propose*** a wafer scale implementation of the MPE. The starting point would be a dedicated processing cell, optimized specifically for the PDE arithmetic and data routing. Because of the relative simplicity of the cell, it is expected that extremely large arrays (8x8 to 32x32) ***could be*** successfully processed on a single piece of silicon using Wafer Scale Integration techniques. In fact, we have already laid the foundation for the development of such a processing cell. Our Universal Multiply-Subtract-Add [11] ***could be*** adapted for this first cell design. Similarly, our nonlinear coprocessor cell [12]-[14] ***might be used*** in conjunction with the UMSA to provide advanced mathematical functions. As suggested in Fig. 2, there would be ***courtyards of processors***, each with two interconnection networks and two memory banks. 2-D, 3-D, and 4-D problems could then be mapped for parallel computations. Since inter-processor delays are very small (say a few ns), extremely high speeds could be achieved. This, together with the high degree of parallelism, would result also in high throughout. We ***envision 100 to 1000 processors (on one wafer) forming a wafer scale MPE***. At a clock frequency of 50 MHz, a single wafer could achieve up to 20 GFLOPs performance. With our nonlinear coprocessor added, each instruction could equate to multiple floating point operations.
>
> Furthermore, because of the extendible architecture, several wafers ***could be*** interconnected as shown in Fig. 5 to construct a "stacked" MPE wafer system (SMPE). Note that no vertical interconnects within the stack of wafers are expected. Tens to hundreds of GFLOPs performance in a volume the size of a desk-top computer [15] ***could*** thus be achieved. However, ***these predictions*** ignore the likely technical advances in the next five years; a tenfold further increase in performance ***might be achievable***. [Emphasis Added]

In response to Applicants' previous arguments that Jain et al represent futuristic and unrealized technology, the examiner invoked "Moore's Law" to assert that the computing capacity of Jain et al would have been available at the time of the invention. The Office Action states that "Applicant has provided no evidence to the contrary."

The attached paper "Tilera Targets Intel, AMD with 100-Core Processor" shows that by 2009 (**six years after** the tine of the present invention) the computing capacity had only at that time reached the 100 processor per wafer threshold capacity described by Jain et al, i.e., "we ***envision*** 100 to 1000 processors (on one wafer) forming a wafer scale MPE." Thus, even if at the time of the invention one of ordinary skill in the art had considered applying the

MPE of Jain et al to solve the computer-encoded differential equations of the first principles simulation model, the computing capacity **specified by** Jain et al would **not** have been available at the time of the invention within a semiconductor device fab.

The Court in *Medichem S. A. v. Rolabo S. L.*, 437 F3d 1157, 77 USPQ2d 1865 (Fed. Cir. 2006) explained that:

> An obviousness determination requires not only the existence of a motivation to combine elements from different prior art references, but also that a skilled artisan would have perceived a reasonable expectation of success in making the invention via that combination.

Accordingly, there is no reasonable expectation of success because a skilled artisan (knowing the unavailability of the Jain et al stacked MPE) would **not** have perceived a reasonable expectation of success of solving (within a device manufacturing fab) computer-encoded differential equations of the claimed first principles physical model concurrently with an actual process being performed and in a time frame shorter in time than the actual process being performed via the combination of Sonderman et al and Jain et al's dedicated MPE.

The only other choice from Jain et al would be to network to geographically distant research and industrial sites in order to implement Jain et al's virtual MPE. See Jain et al's Section IV (reproduced below):

> Networking would be essential to implementation of the virtual MPE as well as in the use of the stacked-wafer MPE by geographically distant research and industrial sites. We present this concept in terms of our home university (University of South Florida); however, they could just as well be presented from another university.

Indeed, this section also suggests that networking to geographically distant research and industrial sites is essential even to the stacked-wafer MPE, even if the stacked-wafer MPE were available at the time of the invention. Accordingly, the combination of combination of Sonderman et al and Jain et al does not fairly teach or suggest solving the computer-encoded differential equations of the claimed first principles physical model

concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed by using code parallelization techniques on multiple simulation modules in the device manufacturing fab, as claimed.

Tan et al provide no teachings to remedy the deficiencies noted above.

Tan et al provide no teachings of a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including a spatially resolved model of a physical geometry of the semiconductor processing tool and a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool.

The most specific teaching in Tan et al regarding their modeling tools appears to be at col. 12, line 63, to col. 13, line 12:

> The APC Framework is designed to integrate with legacy systems such as existing monolithic shop floor control systems. Furthermore, the APC Framework integrates with existing process modeling tools such as Matlab and Matrix-X.
>
> The system functional requirements are derived primarily to support two typical scenarios including run-to-run control, and fault detection and classification. Run-to-run control is a model-based process control that usually involves more than one piece of processing equipment. In a typical usage scenario, the results of material processing at one piece of equipment are passed, or "fed-forward" to a subsequent manufacturing step, and used to influence the future processing of the same material. In the APC Framework, run-to-run control is performed according to mathematical process models, and a single application accommodates multiple feed-forward and feedback loops.

Tan et al, while describing the use of Matlab and Matrix-X for process modeling tools and while describing in general run-to-run control performed according to mathematical process models, fails to disclose or suggest the inputting or the solution of the claimed first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of

the semiconductor processing tool and including a spatially resolved model of a physical geometry of the semiconductor processing tool and a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool.

In the Office Action, the examiner relied on Tan et al for their teaching at col. 2, lines 7-10, of model-based ***real time process control*** using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run. Yet, a "model-based" real time process control does **not** state or anyway describe or suggest that the model is solved concurrently with the actual process being performed, as claimed. Moreover, as noted above, there is no disclosure in Tan et al that the model in their "model-based" control is a first principle physical model (much less a first principle physical model including a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool) or that their model solution was solved in a time frame shorter in time than the actual process being performed. Indeed, the "run-to-run" control of Tan et al would permit additional time to produce "solutions" prior to operating on "a subsequent manufacturing step" or prior to accommodating "multiple feed-forward and feedback loops."

In fact, the record shows that only Applicants have realized that computer-encoded differential equations of the first principles physical model for a spatially resolved model of a physical geometry of the semiconductor processing tool can be solved in a time frame shorter in time than the actual process being performed.

Accordingly, the prior art in combination fails to disclose or suggest or make obvious:

> inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including 1) a spatially resolved model of a physical geometry of the semiconductor processing tool and 2) a grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool;

storing in a fab-level library known simulation results obtained from simulation modules in a device manufacturing fab and distributing the known simulation results to other semiconductor processing tools in the device manufacturing fab;

solving the computer-encoded differential equations of the first principles physical model for a spatially resolved model (including the grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool) concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed by:

using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and

re-using known simulation solutions as initial conditions for the first principles simulation,

wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module;

In particular, Applicants submit that the prior art (even in combination) does not fairly teach nor make obvious the solving of computer-encoded differential equations of the claimed first principles physical model (describing at least one of a basic physical or chemical attribute of the semiconductor processing tool and including a spatially resolved model of a physical geometry of the semiconductor processing tool and including the grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool) concurrently with the actual process being performed and in a time frame shorter in time than the actual process by using in the device manufacturing fab 1) shared known simulations distributed to semiconductor processing tools in the device manufacturing fab and 2) code parallelization techniques on multiple simulation modules in the device manufacturing fab.

Hence, for all of these reasons given above, Claims 1-8, 10, 12-14, 15-30, 32, 35, 35, 37-44, and 48 should be found non-obvious and passed to allowance.

Conclusion: In view of the present amendment and in light of the above discussions, the application as amended herewith is believed to be in condition for allowance.

Respectfully submitted,

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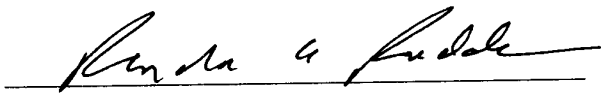

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